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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,082	11/20/2003	Cheng-Sheng Lee	11690-US-PA	1081

31561 7590 11/10/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/707,082	LEE, CHENG-SHENG	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

DETAILED ACTION

1. Applicant's Amendment filed October 06, 2005 has been entered.

2. Claims 1 – 11 are pending.

Response to Arguments

3. Applicant's arguments filed October 06, 2005 have been fully considered but they are not persuasive.

With respect to applicant's remarks, pages 6 – 10, please consider the following respects:

i. Contrary to applicant's assert, claim 1 as presented in the response has **not** been amended.

ii. It is considered non-persuasive to recite the whole claim passage (pages 6 – 7) and conclude that the prior arts do not teach the claimed limitations. Otherwise, this would have been true for all arguments. Applicant should specifically point out which limitation, or feature, one-by-one, in the passage that is not taught, or addressed according to the references.

iii. Contrary to applicant's arguments presented in pages 7 – 8, the references have been cited to teach the limitations required by the claims only. Whether they do not disclose the details as pointed out which differ as compared to the

applicant's specification is not relevant, because the details of how current and/or voltage behave in the circuits are nowhere found in the claims. Claims 1 – 11 only specify the selection signals being on, or off. Applicant should recognize that per the claim language, if a memory device which is shown to behave according to what is claimed, i.e., comprising a column selection line ...; a row selection line ...; and a switch device coupled to the memory cell, ..., it would accordingly be contended to be capable of breaking a leakage current path in a memory array within a memory device, since that is what is claimed.

Applicant please also note that according to the remarks, page 8, lines 8 – 11, *"when at least one of the column selection line and the row selection line does not receive at least one of the column turn-off signal and the row turn-off signal, the power provided from the power supply terminal is coupled to the memory cell,"* it requires that at least one of the selection line does not receive ... turn-off signal, for the power to be coupled to the memory cell. There are two concerns that arise from this limitation.

First, if **both** column selection line and row selection line do not receive the turn-off signal, it also satisfy the requirement of "at least one of..." because the claim did not specify exclusively that one or the other receives the turn-off signal but can not have both to receive the turn-off signal at the same time.

Second, it was interpreted that if the selection line receives the "turn-off signal", it means the line is NOT selected—turn-off. Therefore, if it does not receive the turn-off signal, the line is recognized as "selected", or "addressed", or simply "on". And inherently, when the line(s) are on, power being applied for the selection is only inherent

to one of ordinary skill in the art, because according to the references, these row(s) and/or column(s) lines are directly coupled to the decoders, which apply signals to represent only and either "select" or "non-select", which mean either and only "hi" or "low" according to the address signal. For example, in Sakimura et al., fig. 4 shows an exemplary case when memory cell 2a is selected. This means "at least one of the column selection line and the row selection line does not receive at least one of the column turn-off signal and the row turn-off signal"—in the instance situation, both row and column selection lines do not receive the turn-off signal. And for further clarification, the current Is shown to flow through the memory cell 2a only represents that coupled is coupled to the memory cell. This clearly complies with, and only with, what are claimed.

iv. Contrary to applicant's arguments on page 9 – 10, similar analysis and interpretations as the above also apply with respect to the features as disclosed.

4. The foregoing establishes grounds on which the claims are rejected as follow.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 5, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakimura et al. (US Pat 6,885,579 B2).

Regarding **claims 1 and 7**, Sakimura et al. disclose a device for breaking a leakage current path in a memory array within a memory device (figs. 4, 9, 10, 12a, 12b, or 13) comprising:

a column selection line adapted to select a column of a memory cell within a memory array (fig. 4, line V2');

a row selection line adapted to select a row of the memory cell within the memory array (fig. 4, first power supply line 14, which is line V1); and

a switch device coupled to the memory cell, a power supply terminal, the column selection line and the row selection line (fig. 4, switch devices X-selector 11 and second Y-selectors 13),

wherein when the column selection line receives a column turn-off signal and the row selection line receives a row turn-off signal (exemplary memory cell 2 in a non-selected state—not addressed), the switch device is turned off so that a power provided from the power supply terminal is not coupled to the memory cell (X-selector 11 and the second Y-selector 13, which are not connected to select memory cell 2—open—no closed path for leakage current from memory cell), and when at least one of the column selection line and the row selection line does not receive at least one of the column turn-off signal the row turn-off signal (exemplary memory cell 2a in a selected state—addressed), the power provided from the power supply terminal is coupled to the

memory cell (X-selector 11 connects first power supply line 14 to the selected memory cell 2a, which is also connected to line V2' by the second Y-selector 13, to supply Is to read circuit 16).

Regarding **claims 2 and 8**, Sakimura et al. also disclose the device for breaking the leakage current path of the claim 1 (col. 13, lines 23 – 37), wherein the switch device further comprises:

a first switch coupled to the memory cell, the power supply terminal and the column selection line (fig. 4, second Y-selector 13 couples to selected memory cell 2a, which couples the column selection line V2' to the corresponding column, second column from left, and also couples to receive Is from the first power supply line 14 through the memory cell 2a), wherein when the column selection line receives the column turn-off signal, the first switch is turned off so that the power is not coupled to the memory cell, and when the column selection line does not receive the column turn off signal, the power is coupled to the memory cell;

a second switch coupled to the memory cell, the power supply terminal and the row selection line (fig. 4, X-selector 11 couples the selected memory cell 2a to the first power supply line 14 through the corresponding row), wherein when the row selection line receives the row turn-off signal, the second switch is turned off so that the power is not coupled to the memory cell, and when the row selection line does not receive the row turn-off signal, the power is coupled to the memory cell.

As per **claim 5**, the method for breaking a leakage current path for a circuit having an array disclosed therein is considered inherent given the device as shown above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4, 6, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakimura et al. in view of Arimoto et al. (US Pat Pub 2003/0103368 A1).

Regarding **claims 4, 6, and 10**, Sakimura et al. disclose the device for breaking the leakage current path of claim 1, except wherein the column turn-off signal and the row turn-off signal are controlled by a stand-by signal. However, the feature is taught by Arimoto et al. (paragraph 0645).

Thus, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the feature shown by Arimoto et al. to the disclosure by Sakimura et al., so that current consumed by leakage-defective memory cells can be reduced).

Regarding **claim 11**, Arimoto et al. also disclose the memory device of claim 7, wherein the memory array comprises a DRAM array (paragraph 0036).

9. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakimura et al. in view of Marr (US Pat 6,707,707 B2).

Regarding **claims 3 and 9**, Sakimura et al. disclose the device for breaking the leakage current path of claims 2 and 8, except wherein each of the first switch and the second switch comprises a PMOS transistor or PMOSFET. However, the use of PMOS/PMOSFET as power switch has been taught by Marr (fig. 4, PMOS 82).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature shown by Marr to the specification disclosed by Sakimura et al., to allow signal control for high power switching purposes (col. 4, line 49 – col. 5, line 4).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D. Pham LP
November 2, 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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